IN THE SPECIFICATION

Please replace the paragraph beginning on page 8, line 1, with the following amended version:

--As shown, circuit 120 includes latches 456 and 458 which are configured to receive input data 452. A first circuit 470, a delay locked loop (DLL-1) in the example shown, is coupled to receive input clock signal 454 and output clock signals 459 and 809. Also shown in the embodiment is a system clock signal 802. System clock signal 802, which may be generated locally or globally, is utilized by PLL 472 to generates a clock signal 805 which may generally serve as a reference clock signal. ~~Clock signal 805 is coupled to DLL 1 470.~~ Clock signal 459 is coupled to latches 456 and 458 and is utilized to latch data into latches 456 and 458. Clock signals 805 and 809 are coupled to DLL-2 471 which is further configured to convey clock signal 872 (DLL2_O). Latch outputs FFA 461 and FFB 462 are input to multiplexor 492. Another multiplexor 494 is configured to convey either a logic high or a logic low signal. Clock signal 872 is coupled as a select signal to both multiplexor 492 and 494. Finally, multiplexor 492 is configured to convey output data 496, and multiplexor 494 is configured to convey output clock 498.--

Please replace the paragraph beginning on page 6, line 8, with the following amended version:

--Turning now to Fig. 3, one embodiment of a retiming repeater 150 (alternately referred to as "retiming repeater", "retimer", or "repeater") and its function is illustrated. In the embodiment shown, repeater 150 is configured to receive a source synchronous signal via port 110A from device 507 and transmit a corresponding signal via port 110B. Circuit 120 is configured to control acquisition and transmission of the signals received and transmitted by repeater 150. Illustrated in Fig. 3 are a data line 503 and a clock line 505. A particular length 514 of each line 503 and 505 is indicated. Device 507 transmits signals 502 and 508 via lines 503 and 505 to repeater 150. Initially, signals 502 and 508 have a relatively good degree of integrity with respect to their original amplitude and timing. However, after traveling along the length of lines 503 and 505, signal 504 which corresponds to the original signal 502 has reduced amplitude (is attenuated) and may include jitter. Similarly, signal 510 which corresponds to original signal 508 has reduced amplitude and may include jitter. It is noted that the transmitted data signal 502 and clock signal 508 need not operate at the same frequency. Alternative embodiment may include source synchronous signals wherein the clock signal is either a higher or lower frequency than the corresponding data signal. For example, in one embodiment the transmitted clock signal 508 operates at a fraction of frequency of the data signal 502. In such an

embodiment, the repeater 150 may be configured to multiply the received clock signal 508 in order to match the frequency of the received data signal 502. The multiplied clock signal may then be utilized to capture the received data. Those skilled in the art will appreciate that numerous such alternatives are possible.--

Please replace the paragraph beginning on page 8, line 1, with the following amended version:

--As shown, circuit 120 includes latches 456 and 458 which are configured to receive input data 452. A first circuit 470, a delay locked loop (DLL-1) in the example shown, is coupled to receive input clock signal 454 and output clock signals 459 and 809. Also shown in the embodiment is a system clock signal 802. System clock signal 802, which may be generated locally or globally, is utilized by PLL 472 to generates a clock signal 805 which may generally serve as a reference clock signal. Clock signal 805 is coupled to ~~DLL-1 470~~ DLL-2 471. Clock signal 459 is coupled to latches 456 and 458 and is utilized to latch data into latches 456 and 458. Clock signals 805 and 809 are coupled to DLL-2 471 which is further configured to convey clock signal 872 (DLL2_O). Latch outputs FFA 461 and FFB 462 are input to multiplexor 492. Another multiplexor 494 is configured to convey either a logic high or a logic low signal. Clock signal 872 is coupled as a select signal to both multiplexor 492 and 494. Finally, multiplexor 492 is configured to convey output data 496, and multiplexor 494 is configured to convey output clock 498.--